AMENDMENTS TO THE CLAIMS

1. (Currently Amended) An error correction system for a programmable logic device (PLD), comprising:

a frame circuit arranged to retrieve data from each column of configuration memory of the PLD;

a check memory for storage of a plurality of check words;

a buffer circuit coupled to the check memory and to the frame circuit, the buffer circuit arranged to assemble blocks of data from data retrieved by the frame circuit and from corresponding check words in the check memory;

a mask memory specifying variant memory cells of the configuration memory, wherein a value in a variant memory cell is permitted to vary during operation of the PLD; and

a mask circuit coupled to the mask memory and to the buffer circuit and arranged to substitute in the blocks of data a constant value for the value of each variant memory cell;

a plurality of storage elements; and

a check circuit coupled to the plurality of storage elements and to the buffer circuit, the check circuit arranged to check each block with an error correcting code and store data indicating detected errors in the plurality of storage elements.

Claim 2. (Cancelled)

3. (Currently Amended) The system of claim 1 [[2]], further comprising:

a correction circuit coupled to the check circuit and to the frame circuit, the correction circuit arranged to correct each block found by the check circuit to have an error;

wherein the frame circuit is further arranged to update the configuration memory with a corrected block of data; and

wherein the mask circuit is further arranged to inhibit modification of the value of variant memory cells during updates to the configuration memory with a corrected block of data.

4. (Original) The system of claim 3, wherein the correction circuit is further arranged to update the check memory for the check word corresponding to a block corrected by the correction circuit with a corrected check word for the block.

5. (Original) The system of claim 4, wherein the block ECC is a turbo code.

6. (Original) The system of claim 4, further comprising:

wherein the check circuit is further arranged to calculate a syndrome from the block using a parity check matrix for the block error correcting code and detect a block error from a non-zero syndrome;

wherein the check circuit is further arranged to determine from the syndrome whether a detected error is a correctable error or an uncorrectable error; and

wherein the correction circuit is further arranged to correct a block error that is determined to be a correctable error using the syndrome.

7. (Original) The system of claim 6, wherein the block ECC is a Bose-Chaudhury-Hocquenghem (BCH) code.

8. (Original) The system of claim 7, wherein the BCH code is a 511/528 BCH code.

9. (Original) The system of claim 6, wherein the block ECC is a Reed-Solomon code.

10. (Original) The system of claim 6, wherein the data stored in the plurality of storage elements by the check circuit indicates whether a detected block error is a correctable error or an uncorrectable error.

11. (Original) The system of claim 10, wherein the check circuit is further arranged to indicate in the plurality of storage elements respective numbers of detected correctable errors and detected uncorrectable errors.

12. (Original) The system of claim 1, wherein the check circuit is further arranged to compare a check word from check memory with a check word recalculated from a corresponding block of data, and a difference in comparison indicates a block error.

13. (Original) The system of claim 1, wherein the check circuit is further arranged to calculate a syndrome from a block using a parity check matrix for a block error correcting code, and a non-zero syndrome indicates a block error.

14. (Original) The system of claim 1, wherein the check memory is a portion of the configuration memory.

15. (Original) The system of claim 1, wherein the check circuit is further arranged to periodically check for errors in configuration memory.

16. (Original) The system of claim 1, wherein the frame circuit, check memory, buffer circuit, plurality of storage elements, and check circuit are arranged in a single integrated circuit.

17. (Currently Amended) A method for detection and correction of errors in configuration data of a programmable logic device (PLD), comprising:

retrieving data from each column of configuration memory of the PLD;

specifying variant memory cells of the configuration memory in a mask memory, wherein a value in a variant memory cell is permitted to vary during operation of the PLD;

assembling blocks of data from configuration data retrieved from the columns of configuration memory and from corresponding check words in a check memory;

substituting in the blocks of data a constant value for the value of each variant memory cell;

checking each block with an error correcting code; and

storing data indicative of detected errors in a plurality of storage elements in the PLD.

Claim 18. (Cancelled)

19. (Currently Amended) The method of claim 17 [[18]], further comprising:

correcting configuration data in each block found to have an error;

updating the configuration memory with a corrected block of data; and

inhibiting modification of the value of variant memory cells during updates to the configuration memory with corrected blocks of data.

20. (Original) The method of claim 19, further comprising updating the check memory having the check word corresponding to a corrected block with a corrected check word for the corrected block.

21. (Original) The method of claim 20, wherein the block ECC is a turbo code.

22. (Original) The method of claim 20, further comprising:

calculating a syndrome from the block using a parity check matrix for the block error correcting code and detecting a block error from a non-zero syndrome;

determining from the syndrome whether a detected error is a correctable error or an uncorrectable error; and

correcting a block error that is determined to be a correctable error using the syndrome.

23. (Original) The method of claim 22, wherein the block ECC is a Bose-Chaudhury-Hocquenghem (BCH) code.

24. (Original) The method of claim 23, wherein the BCH code is a 511/528 BCH code.

25. (Original) The method of claim 22, wherein the block ECC is a Reed-Solomon code.

26. (Original) The method of claim 22, wherein the data stored in the plurality of storage elements indicates whether a detected block error is a correctable error or an uncorrectable error.

27. (Original) The method of claim 26, further comprising indicating in the plurality of storage elements respective numbers of detected correctable errors and detected uncorrectable errors.

28. (Original) The method of claim 17, further comprising comparing a check word from check memory with a check word recalculated from a corresponding block of data, wherein a difference in comparison indicates a block error.

29. (Original) The method of claim 17, further comprising calculating a syndrome from a block using a parity check matrix for a block error correcting code, wherein a non-zero syndrome indicates a block error.

30. (Original) The method of claim 17, wherein the check memory is a portion of the configuration memory.

31. (Original) The method of claim 17, further comprising periodically performing the steps to retrieving, assembling, checking, and storing.